Digital Five Band Equaliser with Linear Phase

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Abstract

A five band digital equaliser with linear phase was implemented in a 24 bit DSP. A multirate tree filter bank not maximally decimated was used to reduce the required processing power. Taking advantage of certain filter symmetries and with careful filter design, a very efficient algorithm was implemented. The frequency resolution of this equaliser is better than the analogue counterparts, and the listening tests showed good results.

1 Introduction

The analogue graphic equalisers are usually made with parallel connected band-pass filters centred around the control frequencies. The trade off between the central frequency and the bandwidth, has to be carefully chosen to avoid excess of ripple in the frequency response. Second order filters are usually used to avoid excess of phase distortion, therefore, the frequency selectivity is very poor. It is possible to improve the ripple in the frequency response and eliminate the phase distortion by using linear phase digital FIR filters. Although the phase distortion is not perceived by the human ear, it is important in stereo image definition. The introduction of digital signal processing techniques in the HI-FI systems is very pertinent because of the raising market of digital audio supports as CD[1], DAT[2], and broadcasting as the DSR[3] and DAB[4]. Several manufacturers have seen this market as a potential one and designed low cost DSP with special functions appropriated to digital audio applications.

In this paper we describe a five band digital equaliser that solved most of the draw backs of the analogue counterparts. Therefore we used a multirate filter bank with linear phase frequency response and a very good frequency selectivity. The penalty to this better performance, is the greater group delay of this equaliser (40ms), and the cost of the DSP system.

2 System Architecture

The proposed equaliser could have been done using an architecture similar to the analogues versions, what is, several linear phase FIR filters connected in parallel. However, as can be easily verified, the filter size for the lowest frequency band would be prohibitive. A possible solution to process those large filters could have been the use of special hardware and algorithms which made the filter processing using circular convolution with FFT and the "overlap and add" or the "overlap and save" algorithms[1-2]. To avoid the use of special hardware we had to search for an alternative. Some works on digital equalisers with multirate filter banks [3-6] and a large number of recent works on multirate filter banks [7-16], led us to the proposed solution. As can be observed in fig.1, a tree structured filter bank was used with only three different decimation and interpolation filters. The analysis filter bank was made of four equal stages that splits the input signal in two bands. The output of the high-pass filter (*HP*1) becomes in each stage one of the equaliser bands. The lower band is decimated by three and passed to the next stage. The synthesis filter bank has to recombine the five

[1] Compact Disk.

[2] Digital Audio Tape.

[3] Digital Satellite Radio.

[4] Digital Audio Broadcasting.

bands signals by doing the appropriate interpolation and filtering, to eliminate the imaging effect. The frequency response of the analysis filter bank (*LP*1 and *HP*1) and of the synthesis filter bank (*LP*2) is shown in fig.2.

In order to obtain an overall flat frequency response, the filters *LP*1 and *HP*1 must be symmetric around the middle of the transition band frequency f_3 (fig.2), or equivalently the filters frequency response must satisfy the equation $|LP1|+|HP1|=1$. If this condition is hold, to avoid interference in the symmetry of the filters *LP*1 and *HP*1 the pass-band cut-off frequency f_2 of *LP2* must be greater or equal to the stop-band cut-off frequency ω_1 of *LP1*.

As proved in the appendix A it is not possible to do equalisation and maintain the perfect reconstruction characteristic at the same time with maximally decimated filter banks. We have to use sub-maximally decimated filter banks where the cut-off frequency of the decimation filter *LP1* is smaller than $f_1 \le f_s/2D$, where D=3 is the decimation factor and f_s=44,1KHz is the sampling rate. This frequency can be chosen arbitrarily but the bandwidth of the transition band can only be twice de space between f_1 and $f_s/2D$ so that the imaging effect in interpolation filter is avoid.

To design the filters with an attenuation of 90dB in the rejection band, we have used an optimisation program [5] that gives the smaller filter for a given frequency response specification.

The impulse response of the equaliser is approximately a dirac impulse when all the gains C_i in the bands are equal. The frequency response and the impulse response of the equaliser for C_i =1, is draw in fig.3 and fig.4 respectively. As can be seen the filters were designed in a way that the ripple of the overall frequency response is less than 0.2dB. An example of frequency response is given in fig.5 with the control settings at C_i=[0; -10; 0; 0; +12]dB.

The overall delay of the equaliser is give by the expression

$$Delay = \left(\frac{N_{LP1}-1}{2} + \frac{N_{LP2}-1}{2}\right) \times \frac{D^{N-1}-1}{D-1} - \frac{N_{HP1}-1}{2},$$

where N is the number of bands of the equaliser N_{LP1}=39, N_{LP2}=51 and N_{HP1}=39 are the size of the filters *LP*1, *LP*2 and *HP*1 respectively. The total delay with those filter sizes is 40ms. The previous equation shows one of the major drawbacks of this type of structure, that is the delay grows as D^N. For a 10 bands equaliser the total delay would be 9,8s.

3 DSP Implementation

This digital equaliser was implemented on a 24 bit fixed point DSP. This chip has a very good ratio performance/price but it has limited internal memory resources and a very slow interface with the external memory. Due to this the delay buffers (see in Fig.1 Delay1-4) had to be stored on the external memory.

The overall processing architecture was based in the work of [6], and our specific implementation for one channel is described in fig.7. In this figure we only show the first two decimation and interpolation stages from a total of four. The processing is interrupt driven and in each interruption one or two of the stages is ran. As mentioned before, the *LP*1 filter is a mirror version of the *HP*1 filter, so we have $|H_{LP1}| = 1 - |H_{HP1}|$, or in the time domain

$$h_{LP1}(n) = h_{HP1}\left(\frac{N_{HP1}-1}{2}\right) - h_{HP1}(n) \quad ; n = 0..N_{HP1}-1.$$

Using this filter property the overhead to obtain the output of the low-pass filter is minimal (one addition more), due to this and to simplify the software, the output of *LP*1 is evaluated at the same rate as the high-pass filter and then decimated, see fig.7.

4 Evaluation System and Results

To evaluate the quality of this equaliser with some listening tests, it was developed another version of the proposed equaliser on a PC DSP card. A DLL[5] was build to allow windows programs to communicate with the DSP, and an user interface was developed to allow an easy control of the equaliser in real time. The equaliser behaves very well when we move the slider, without any audible clicks. The frequency selectivity is very sharp and the sound is very good even when we raise very much a band.

Appendix A

To verify that it isn't possible to obtain perfect alias cancellation with maximally decimated filter banks when we want to equalise a digital signal, we are going to analyse the two band case. The filter bank in fig.6 splits the input signal *X*(z) in two and its transfer function is given by the following equation:

$$\begin{aligned} T(z) = &\frac{1}{2}\left\{K_1(z)C_1H_1(z) + K_2(z)C_2H_2(z)\right\}X(z) + \\ &\frac{1}{2}\left\{K_1(z)C_1H_1(-z) + K_2(z)C_2H_2(-z)\right\}X(-z) \end{aligned} \tag{1}$$

To have alias cancellation the second term of (1) should be zero. This can be achieved if the following filter relations are verified:

$$K_1(z) = H_1(z) \qquad\qquad K_2(z) = -H_2(z) = -H_1(-z)\,. \tag{2}$$

Then (1) becomes:

$$\begin{aligned} T(z) = &\frac{1}{2}\left\{C_1H_1^2(z) - C_2H_1^2(-z)\right\}X(z) + \\ &\frac{1}{2}\left\{\left[C_1 - C_2\right]H_1(z)H_1(-z)\right\}X(-z) \end{aligned}. \tag{3}$$

As we can see, only when $C_1 = C_2$ the second term in (3) is zero and the aliasing is perfectly cancelled, leading to the equation

$$T(z) = \frac{C_1}{2}\left\{H_1^2(z) - H_1^2(-z)\right\}X(z)\,. \tag{4}$$

The system transfer function *T*(*z*) would get the form $T(z) = Cz^{-K_0}$, where K_0 is a constant delay, if the filters $H_1(z)$ and $H_2(z)$ are power complementary $\left|H_1(z)\right|^2 + \left|H_2(z)\right|^2 = 1$.

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Figures

Fig.1 - Block diagram describing the processing done in the proposed equaliser.

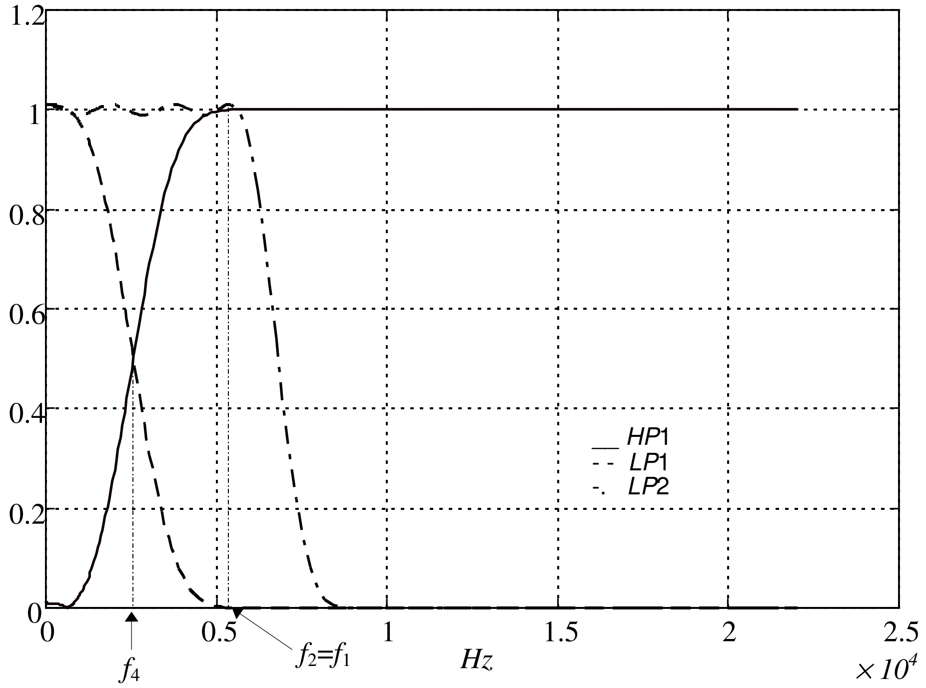

Fig.2 - Frequency response of the decimation filter *LP*1, the high-pass filter *HP*1 and the interpolation filter *LP*2. The sampling rate is f_s=44,1KHz and the decimation factor *D*=3.

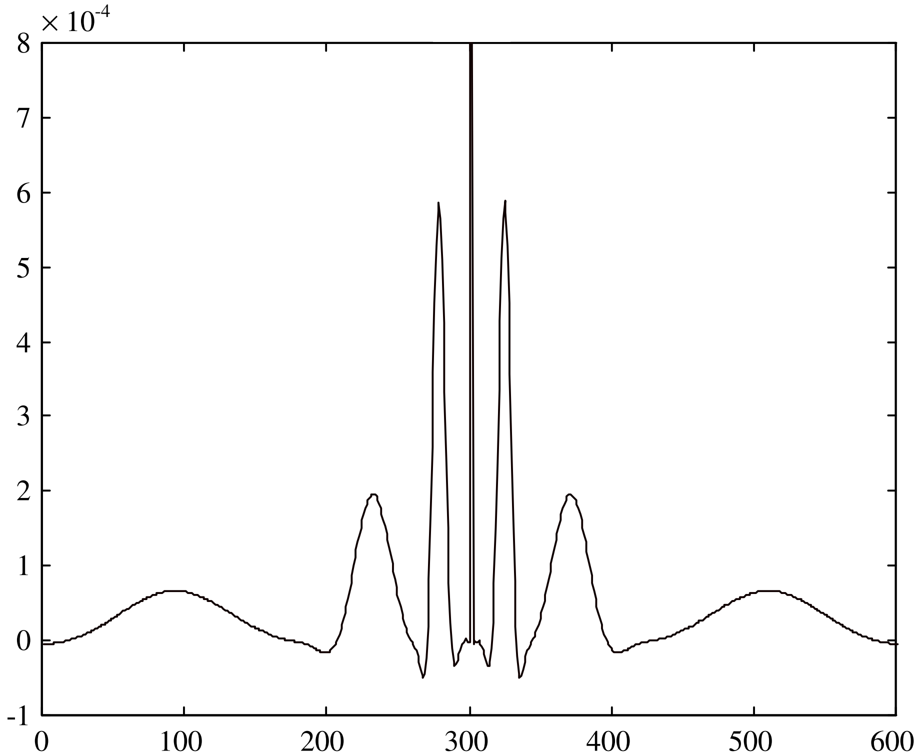

Fig.3 - Equaliser impulse response when all the gains are equal to one $C_i = 1$ (0dB). Note that the vertical axis is scaled to shown the differences to the ideal impulse.

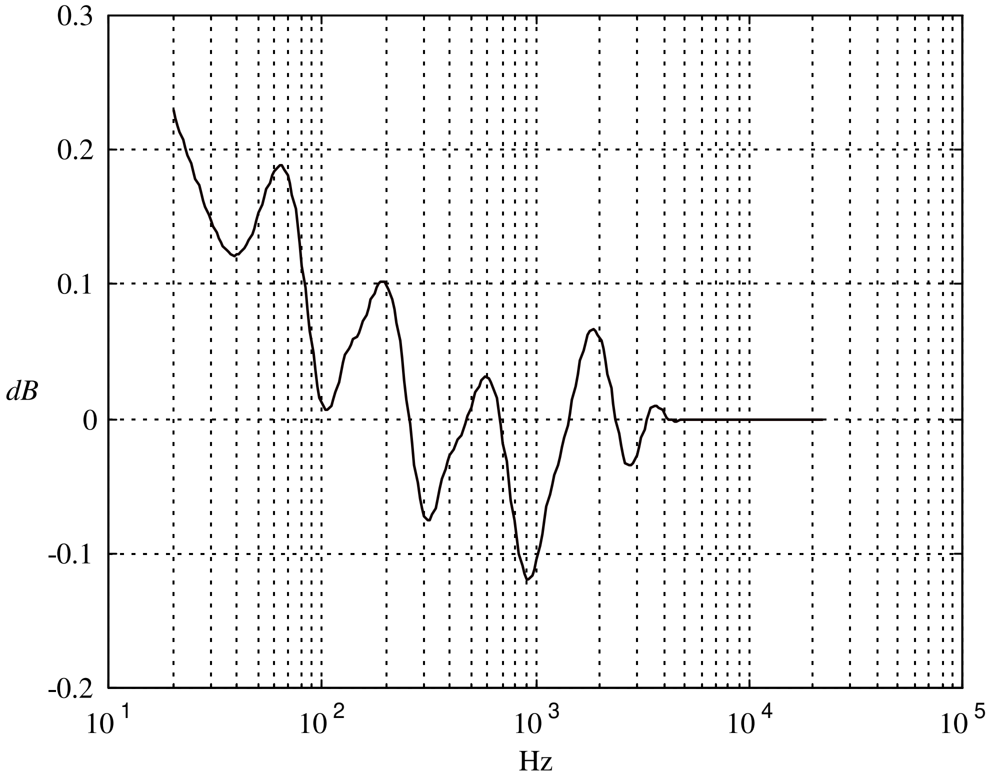

Fig.4 - Equaliser frequency response when all the gains are equal to one $C_i = 1$ (0dB).

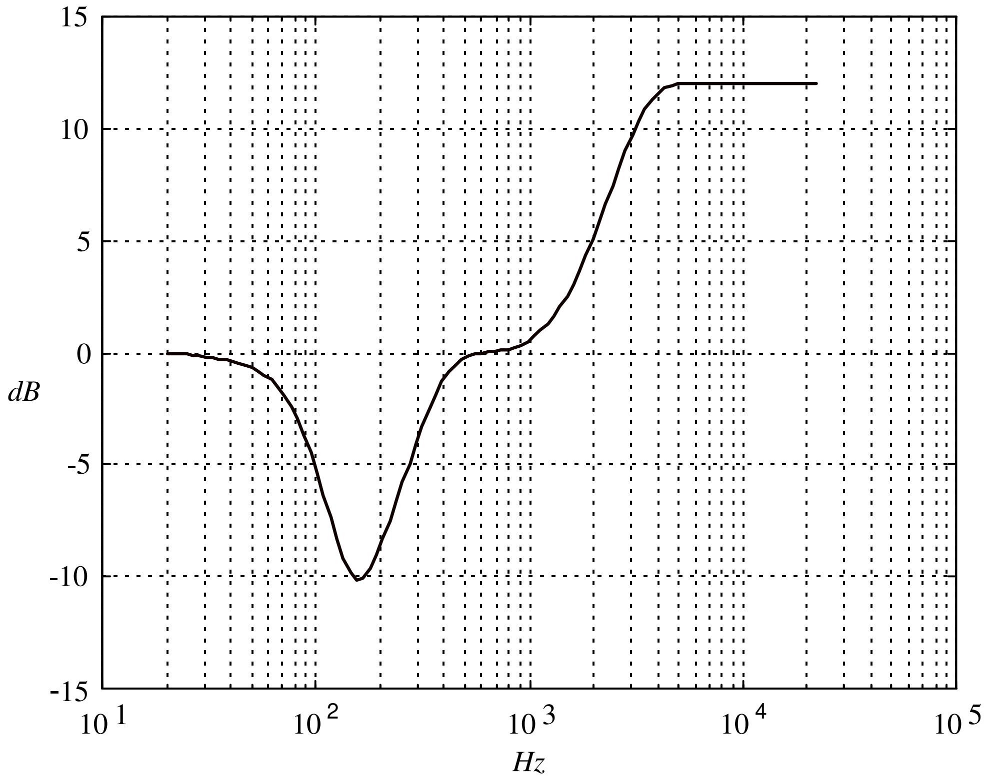

Fig.5 - Equaliser frequency response when the band gains have the following configuration: C_i=[0; -10; 0; 0; +12]dB.

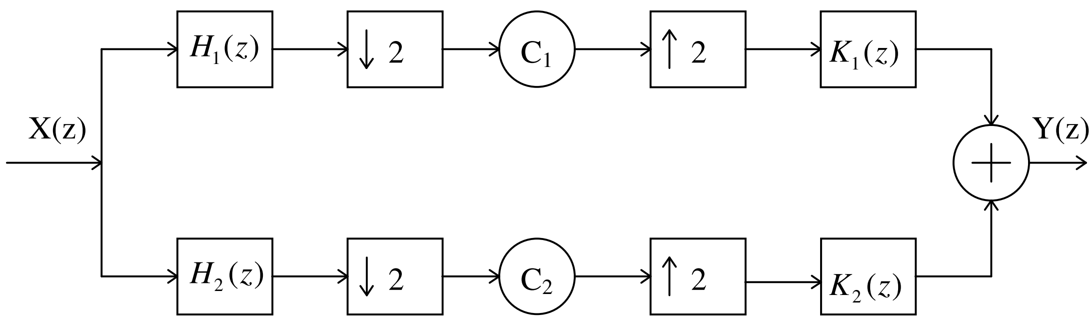

Fig.6 - Maximally decimated two band filter bank.

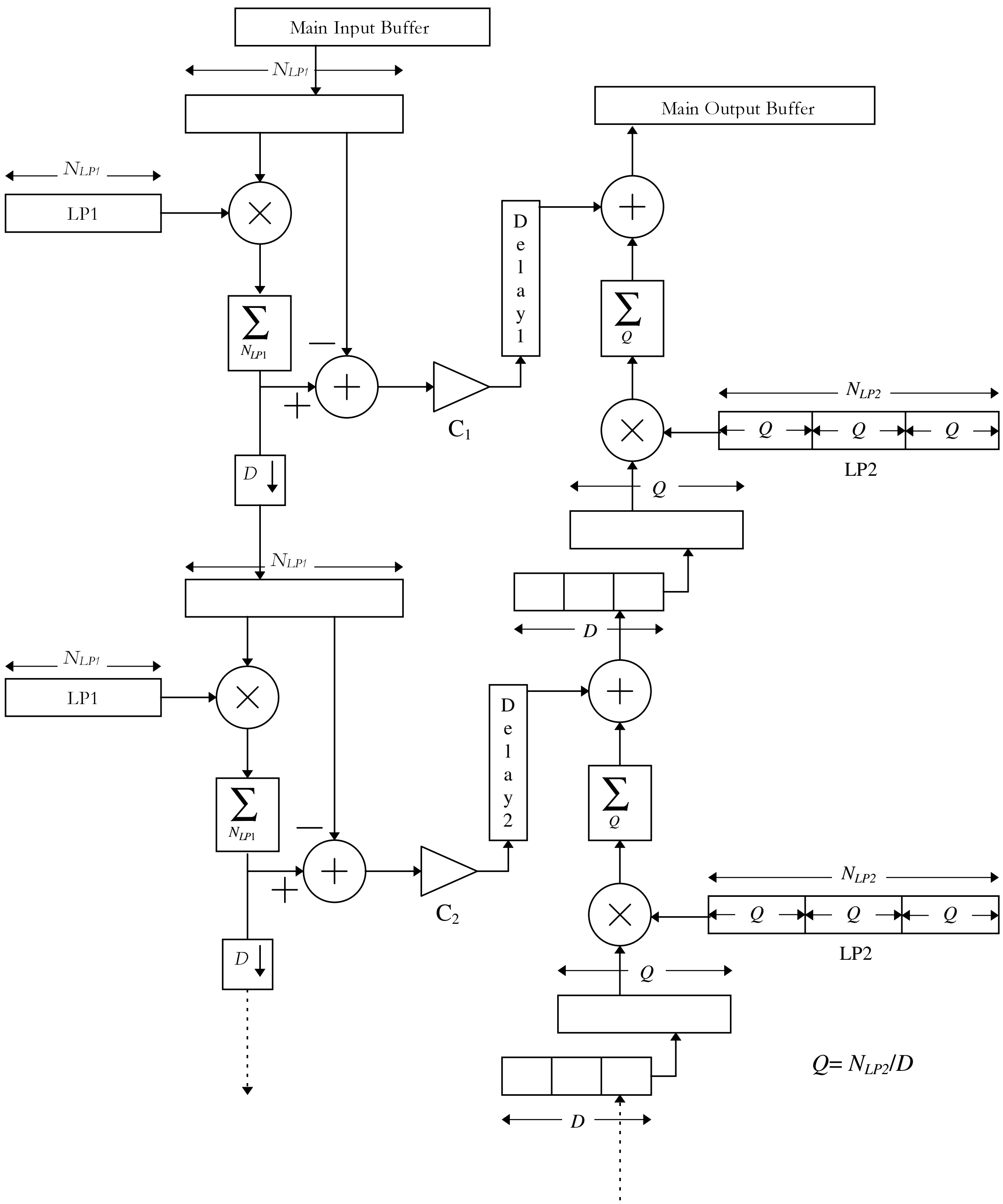

Fig.7 - Detailed description of system architecture. We can see on the left two of the four decimation stages and on the left two of the four interpolation stages.