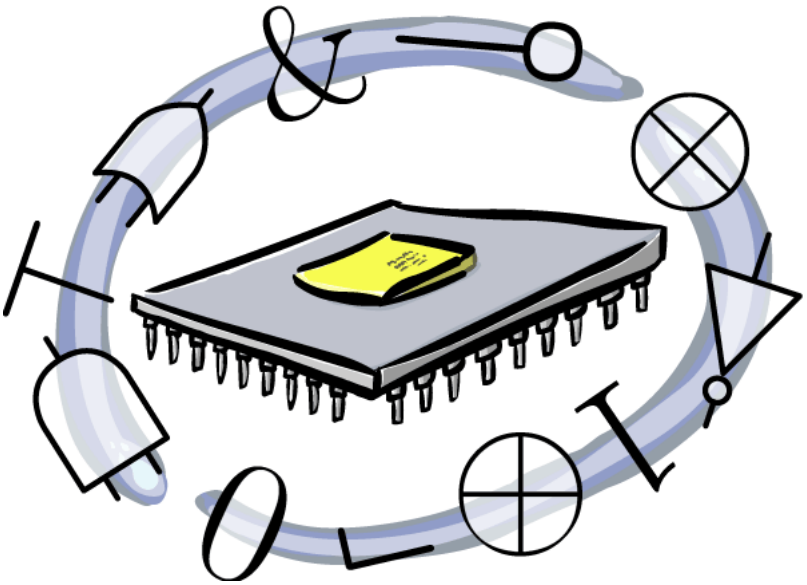


SISTEMAS DIGITAIS RECONFIGURÁVEIS

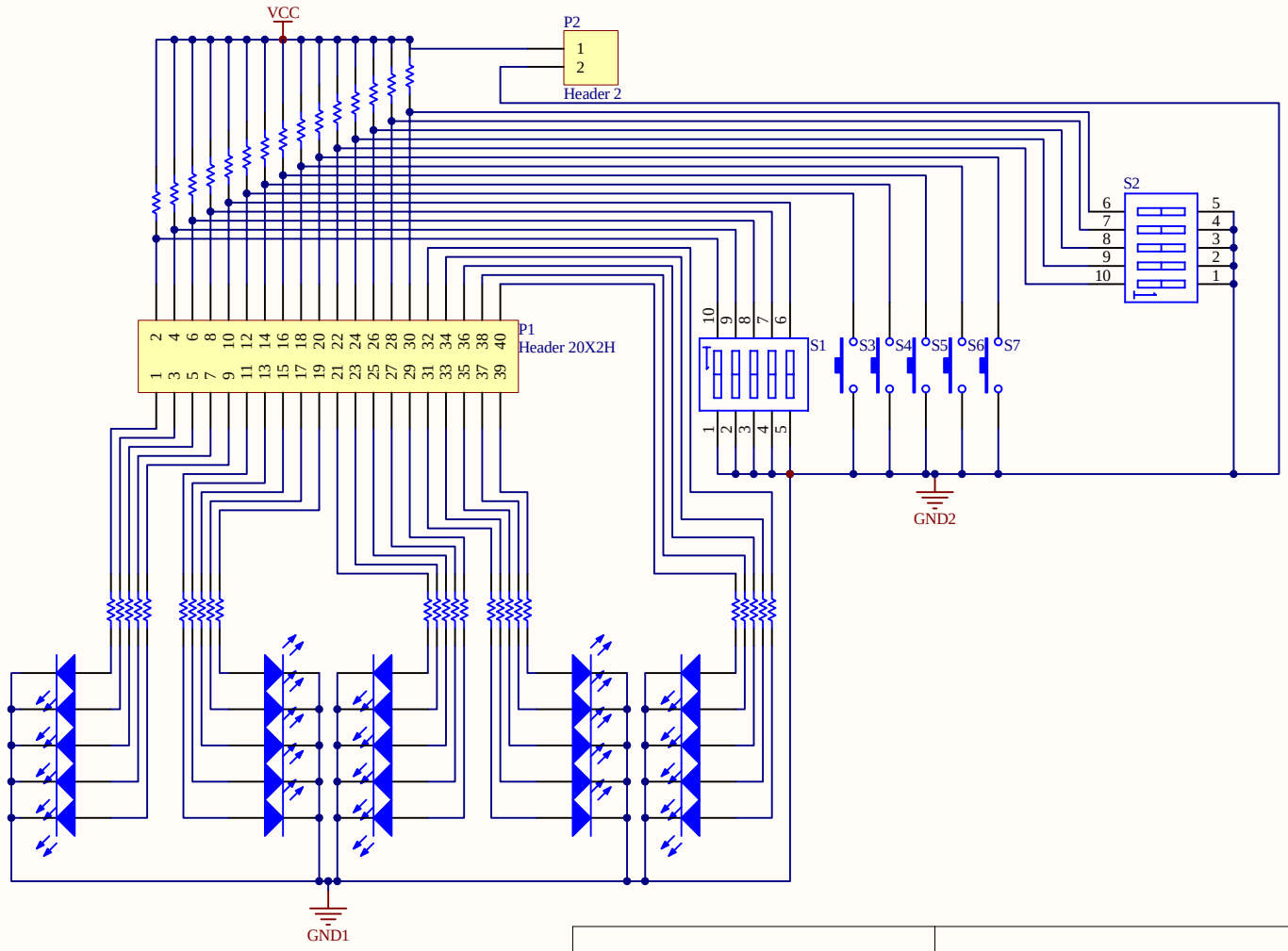
2006/2007 - 1o Semestre

João Fernandes NMEC 22166

22 de Novembro de 2006

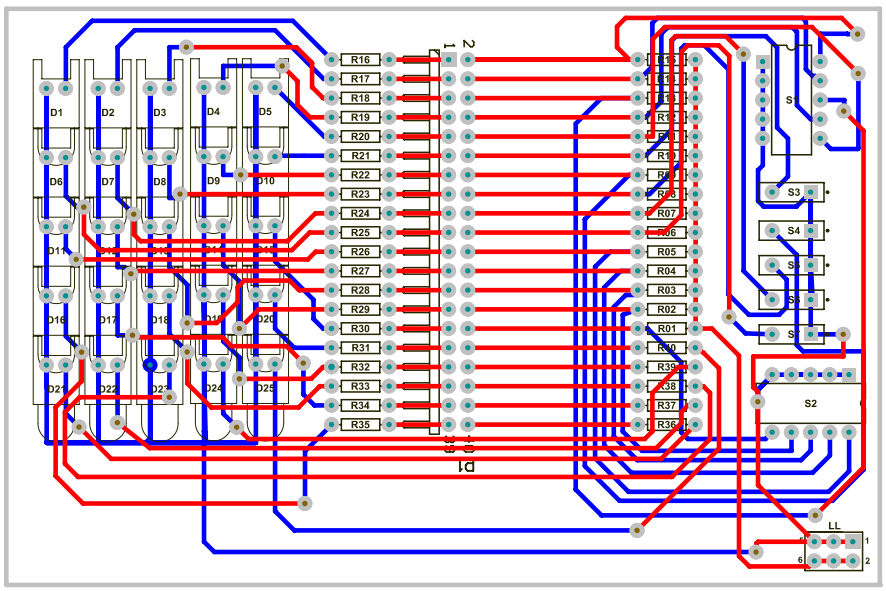
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Projecto is
Port (  rst : in std_logic;
       clk : in std_logic;
       L1 :  out std_logic_vector(1 to 5);
       L2 :  out std_logic_vector(1 to 5);
       L3 :  out std_logic_vector(1 to 5);
       L4 :  out std_logic_vector(1 to 5);
       L5 :  out std_logic_vector(1 to 5);
       S1 :  in std_logic_vector(1 to 5);
       S2 :  in std_logic_vector(1 to 5);
       B :   in std_logic_vector(1 to 5));
end Projecto;
architecture Behavioral of Projecto is
signal LL1, LL2, LL3, LL4, LL5: std_logic_vector (1 to 5);
begin
   process (clk)
      begin
         if (rst='0') then
              LL1<=(others=>'0');
             LL2<=(others => '0');
             LL3<=(others => '0');
             LL4<=(others => '0');
             LL5<=(others => '0');
         else
             if (B(1)='0') then
                if ((S1="11111") or (S2="11111")) then
                    LL1<=(others => '0');
                    LL2<=(others => '0');
                    LL3<=(others => '0');
                    LL4<=(others => '0');
                    LL5<=(others => '0');
               else
                    for c in integer range 1 to 5 loop –coluna
                     if (S2(c)="0") then
                       for i in integer range 1 to 5 loop --linha
                           if (S2(1)='0') then
                                  LL1(c)<='1';
                           end if;
                           if (S2(2)='0') then
                                  LL2(c)<='1';
                           end if;
                           if (S2(3)='0') then
                                  LL3(c)<='1';
                           end if;
                           if (S2(4)='0') then
                                  LL4(c)<='1';
                           end if;
                           if (S2(5)='0') then
                                  LL5(c)<='1';
                           end if;
                      end loop;
                   end if;
                  end loop;
             end if;
      end if;
     end if;
   end process;
   L1<=LL1;
   L2<=LL2;
   L3<=LL3;
   L4<=LL4;
   L5<=LL5;
end Behavioral;
```

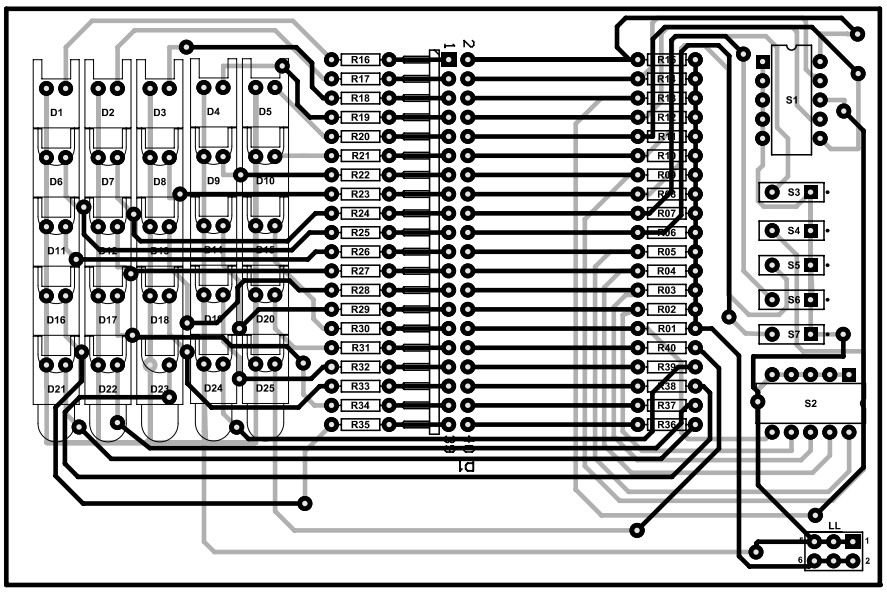
```
1  NET "clk80" LOC = "p79";
2
3  NET "clk80" TNM_NET = "clk80";
4  TIMESPEC "TS_clk80"=PERIOD "clk80" 80 MHz HIGH 50 %;
5
6  #Linha 1
7  NET "L1<1>" LOC = "P106";
8  NET "L1<2>" LOC = "P108";
9  NET "L1<3>" LOC = "P111";
10 NET "L1<4>" LOC = "P114";
11 NET "L1<5>" LOC = "P116";
12 #Linha 2
13 NET "L2<5>" LOC = "P119";
14 NET "L2<4>" LOC = "P122";
15 NET "L2<3>" LOC = "P124";
16 NET "L2<2>" LOC = "P126";
17 NET "L2<1>" LOC = "P130";
18 #Linha 3
19 NET "L3<1>" LOC = "P132";
20 NET "L3<2>" LOC = "P135";
21 NET "L3<3>" LOC = "P138";
22 NET "L3<4>" LOC = "P140";
23 NET "L3<5>" LOC = "P143";
24 #Linha 4
25 NET "L4<5>" LOC = "P146";
26 NET "L4<4>" LOC = "P148";
27 NET "L4<3>" LOC = "P150";
28 NET "L4<2>" LOC = "P154";
29 NET "L4<1>" LOC = "P156";
30 #Linha 5
31 NET "L5<5>" LOC = "P147";
32 NET "L5<4>" LOC = "P149";
33 NET "L5<3>" LOC = "P152";
34 NET "L5<2>" LOC = "P155";
35 NET "L5<1>" LOC = "P161";
36 #switch 1
37 NET "S1<5>" LOC = "P107";
38 NET "S1<4>" LOC = "P109";
39 NET "S1<3>" LOC = "P113";
40 NET "S1<2>" LOC = "P115";
41 NET "S1<1>" LOC = "P117";
42 #Botões
43 NET "B<5>" LOC = "P120";
44 NET "B<4>" LOC = "P123";
45 NET "B<3>" LOC = "P125";
46 NET "B<2>" LOC = "P128";
47 NET "B<1>" LOC = "P131";
48 #switch 2
49 NET "S2<5>" LOC = "P133";
50 NET "S2<4>" LOC = "P137";
51 NET "S2<3>" LOC = "P139";
52 NET "S2<2>" LOC = "P141";
53 NET "S2<1>" LOC = "P144";
```



Size	FCSM No.	DWG No.	Rev
A4			

Scale		Sheet


D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R08
R07
R06
R05
R04
R03
R02
R01
R00
R39
R38
R37
R36
D1
S1
S3
S4
S5
S6
S7
S2
LL


D1
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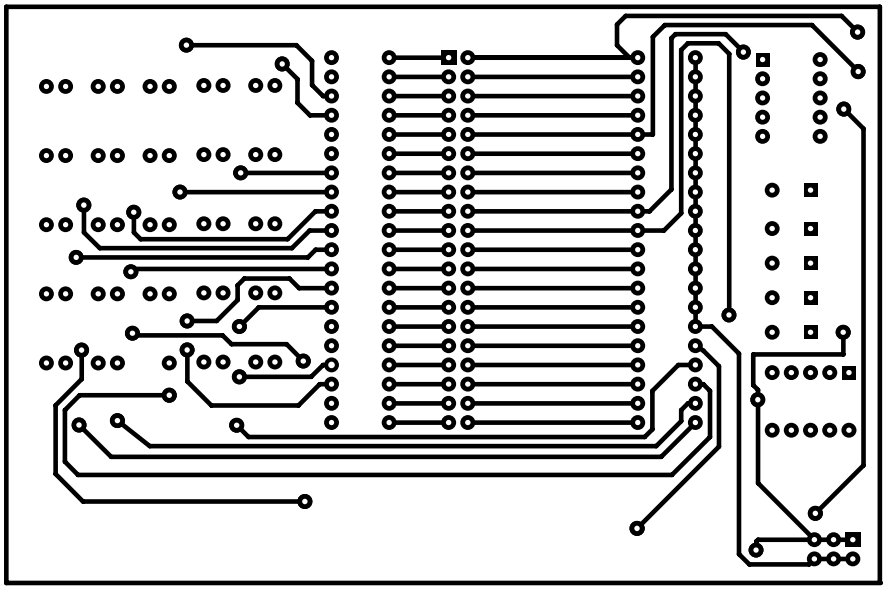
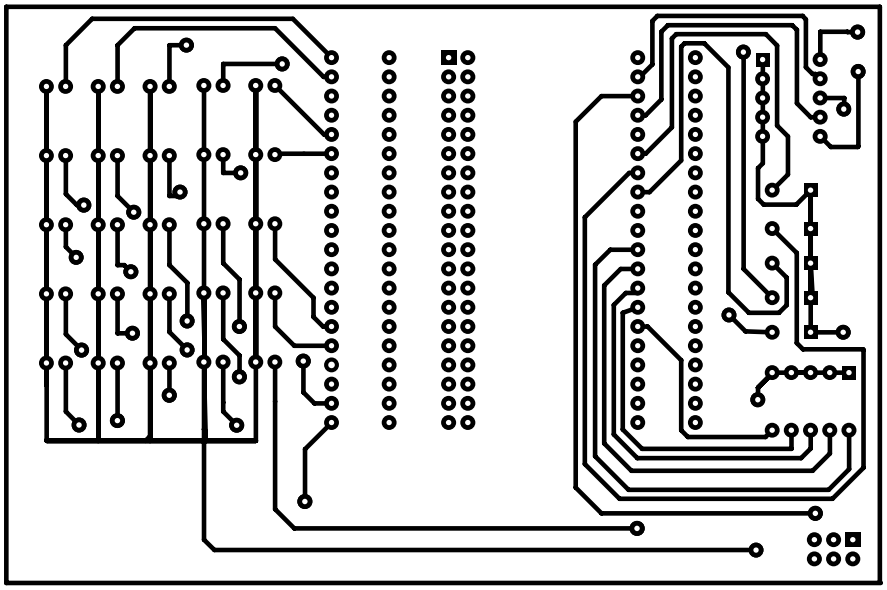
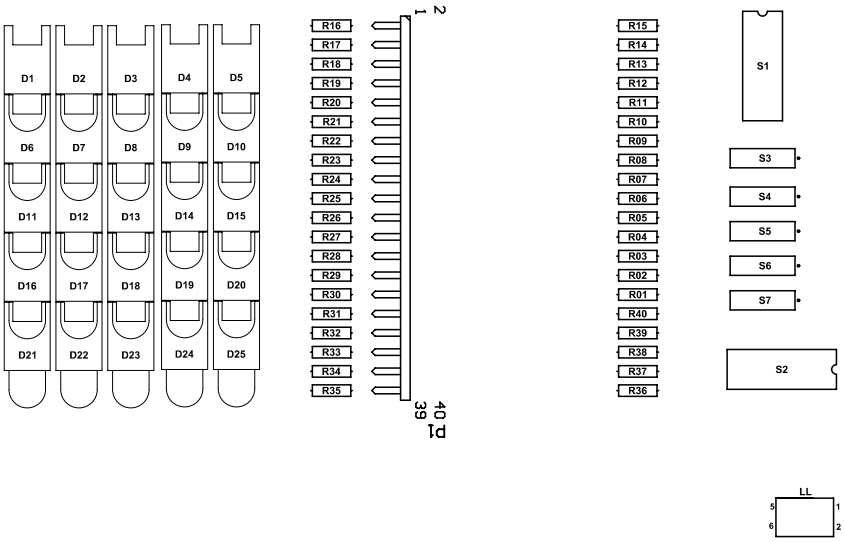
D11
D16
D17
D18
D20
D21
D22
D23
D24
D25
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R01
R02
R03
R04
R05
R06
R07
R37
R38
R40
S1
S3
S4
S5
S6
S7
S2
LL
P1






D1
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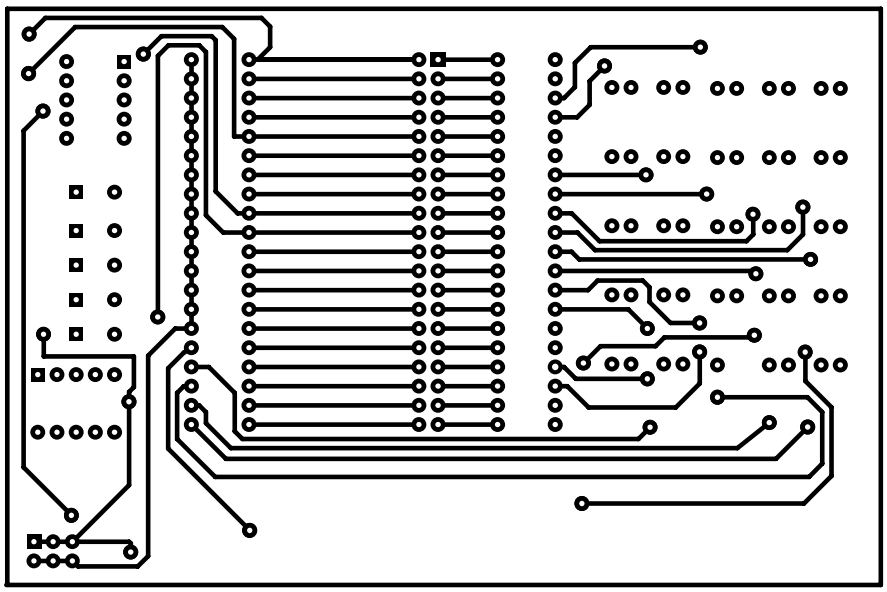
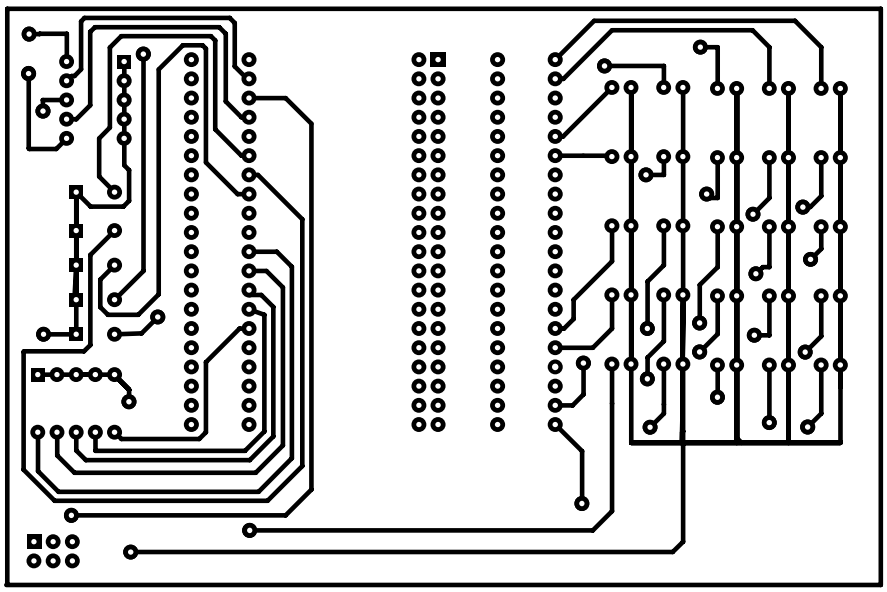
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
2
1
40
39
P1
R15
R14
R13
R12
R11
R10
R09
R08
R07
R06
R05
R04
R03
R02
R01
R40
R39
R38
R37
R36
S1
S3
S4
S5
S6
S7
S2
LL
5
6
1
2





Comment	Description	Designator	Footprint	LibRef	Quantity	Ref
LED0	Typical INFRARED GaAs LED	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25	LED-0	LED0	25	LED 1.5/2.4 V
Header 20X2H	Header, 20-Pin, Dual row, Right Angle	P1	HDR2X20H	Header 20X2H	1	Ficha 40 PIN
Header 2	Header, 2-Pin	P2	HDR1X2	Header 2	1	2 Pins De Alimentação
Res1	Resistor	R16, R17, R18, R19, R20, R21, R22, R23, R24, R25,R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40	AXIAL-0.3	Res1	25	Resistencia diodos
Res1	Resistor	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15	AXIAL-0.3	Res1	15	Resistencia Switch's
SW DIP-5	DIP Switch, 5 Position, SPST	S1, S2	N10A	SW DIP-5	2	DIP Switch 5
SW-PB	Switch	S3, S4, S5, S6, S7	SPST-2	SW-PB	5	Botão de Persão

FPGA	BOARD	FICHA		FPGA	BOARD	FICHA
#Linha 1				#Linha 5		
P106	LED 1	1		P147	LED 21	32
P108	LED 2	3		P149	LED 22	34
P111	LED 3	5		P152	LED 23	36
P114	LED 4	7		P155	LED 24	38
P116	LED 5	9		P161	LED 25	40
#Linha 2				#switch 1 Colunas		
P119	LED 6	11		P107	C 1	2
P122	LED 7	13		P109	C 2	4
P124	LED 8	15		P113	C 3	6
P126	LED 9	17		P115	C 4	8
P130	LED 10	19		P117	C 5	10
#Linha 3				#Botões		
P132	LED 11	21		P120	B 1	12
P135	LED 12	23		P123	B 2	14
P138	LED 13	25		P125	B 3	16
P140	LED 14	27		P128	B 4	18
P143	LED 15	29		P131	B 5	20
#Linha 4				#switch 2 Linhas		
P146	LED 16	31		P133	L 1	22
P148	LED 17	33		P137	L 2	24
P150	LED 18	35		P139	L 3	26
P154	LED 19	37		P141	L 4	28
P156	LED 20	39		P144	L 5	30

VISTA 3D DA BOARD

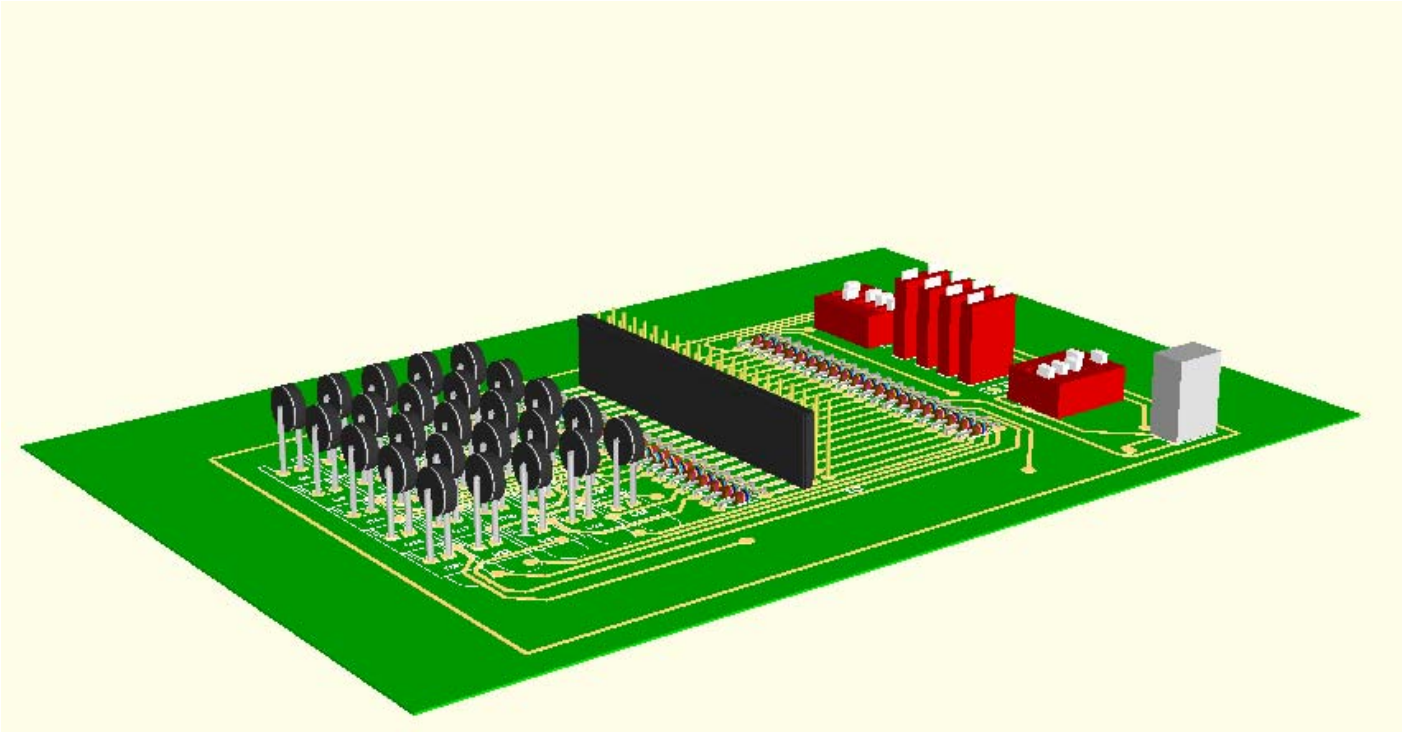


Fig.1 Vista 3D Top

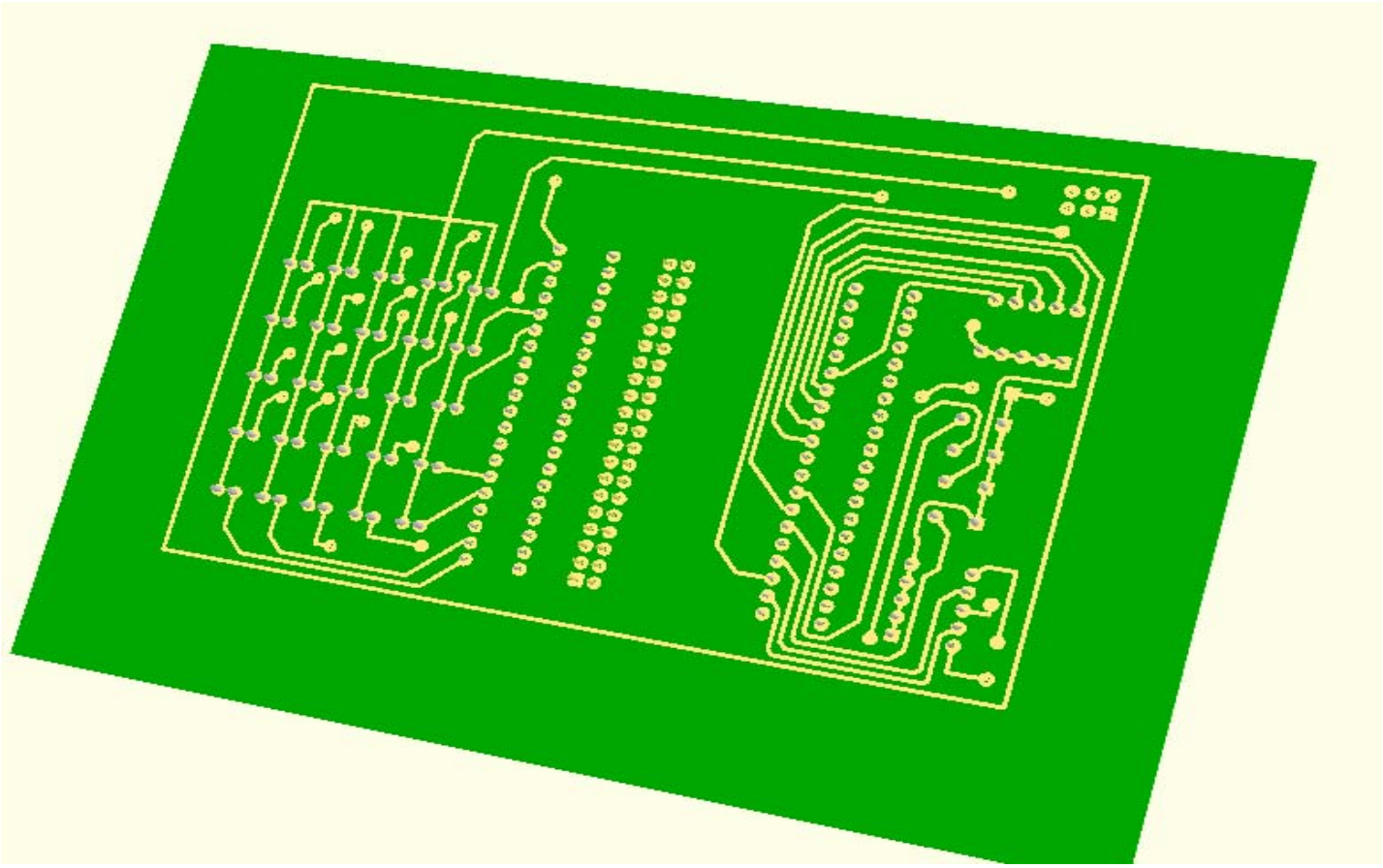


Fig.2 Vista 3D Bottom