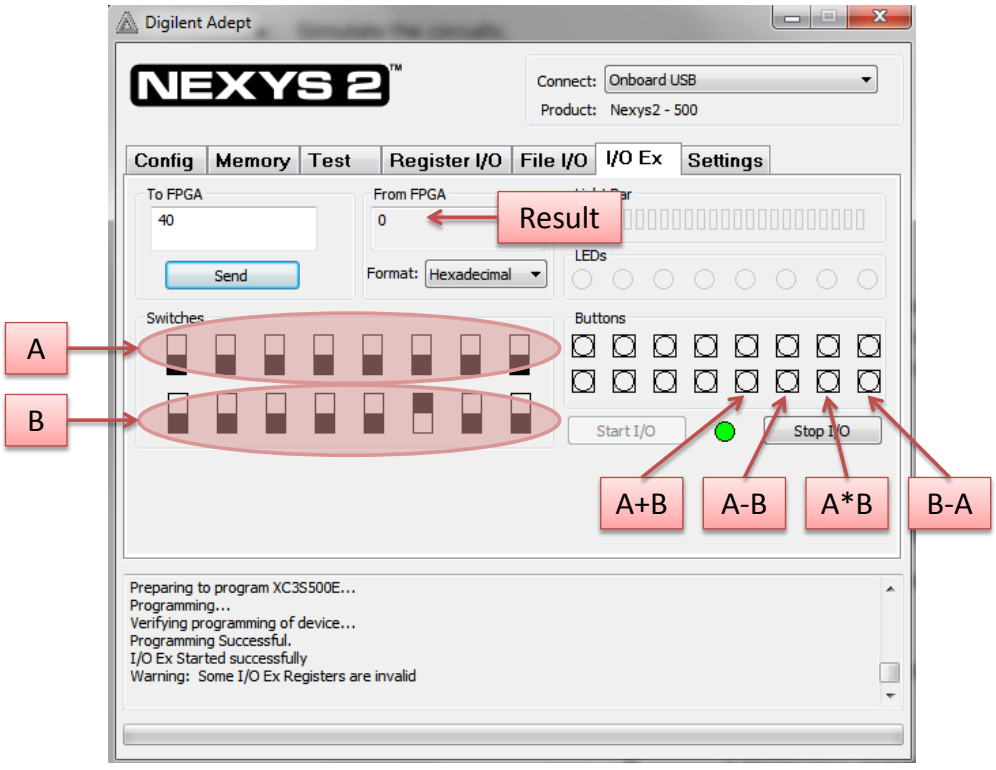
LAB.

Objectives

- Become familiar with Adept I/O interface;
- Update knowledge in VHDL (behavioral and structural specifications, concurrent and sequential statements, processes, data types and operations);
- Describe simple combinational circuits using VHDL;
- Specify sorting networks in VHDL;
- Create parameterizable circuits;
- Simulate the circuits;
- Synthesize and implement the designs;
- Test the circuits in FPGA.

Task 1

Implement a circuit which executes simple arithmetical operations over two unsigned 8-bit numbers A and B. The numbers are specified with the aid of virtual switches, the operation to execute is selected with virtual buttons, and the result is sent to PC and displayed in “From FPGA” field:



Task 2

Describe in VHDL an even-odd transition network which sorts 8 16-bit numbers in ascending order. Start with creating a constant set (array) of numbers to sort and construct the fixed network of comparators. Simulate your design.

Synthesize, implement, and test your circuit in FPGA. Check the results by getting the sorted numbers one by one through I/O Ex.

Try to design a parameterizable even-odd transition network which sorts N M-bit numbers in ascending order. Discover the maximum number of N which is implementable in the target FPGA (for M = 32).

Pipeline your designs. Evaluate the occupied resources and the maximum attainable clock frequency in different implementations.