LAB. 1

Objectives

- Become familiar with Xilinx ISE;
- Update knowledge in VHDL (behavioral and structural specifications, concurrent and sequential statements, processes, data types and operations);
- Describe simple combinational circuits using VHDL and schematics;
- Understand design hierarchy;
- Simulate the circuits;
- Become familiar with the prototyping boards;
- Synthesize and implement the design;
- Test the circuits in FPGA.

Task

Implement a modulo-16 down counter (generates the following sequence of states: 0, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, 15, …) which operates at a frequency of 1 Hz and has a synchronous reset. Display the result of counting in hexadecimal format on a 7 segment display available on the prototyping board.

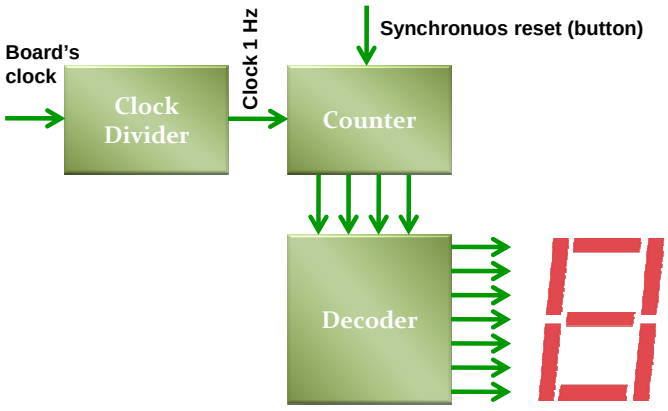
Details

1. Decompose your circuit into 3 components (shown on figure below):

a) Clock Divider – generates 1Hz clock from board's clock signal;

b) Counter – performs counting operation as requested;

c) Decoder – indicates which segments to illuminate on a 7 segment display for each given 4-bits binary value.



2. Describe the functionality of all the components in VHDL. Use design templates if required.

3. Connect all the components using either schematics or VHDL.

4. Write a test bench and simulate the resulting circuit.

5. Assign the external circuit inputs/outputs to the relevant FPGA pins (consult the board's documentation).

6. Synthesize, implement, and test your circuit in FPGA.